Clock OSC

SG-210STF

SG-210STF 25.000000 MHz L Product name Product Number / Ordering code

X1G0041710033xx

Please refer to the 8.Packing information about xx (last 2 digits)

Output waveform CMOS

Pb free / Complies with EU RoHS directive

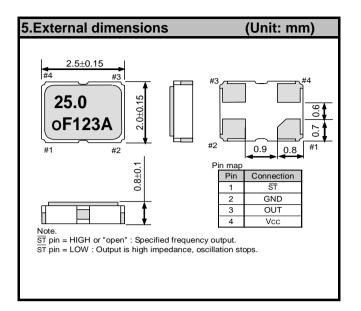
Reference weight Typ. 12 mg

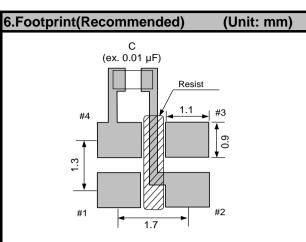
1.Absolute maximum ratings						
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions / Remarks
Maximum supply voltage	Vcc-GND	-0.3	-	+4	V	-
Storage temperature	T_stg	-40	-	+125	°C	Storage as single product
Input voltage	Vin	-0.3	-	Vcc+0.3	V	ST terminal

2.Specifications(characteris	tics)					
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions / Remarks
Output frequency	fO		25.000000		MHz	
Supply voltage	Vcc	1.6	-	3.6	V	-
Operating temperature	T_use	-40	-	+85	°C	-
Frequency tolerance	f_tol	-50	-	50	x10 ⁻⁶	T_use
Current consumption	lcc	-	-	2.2	mA	No load condition Vcc = 3.6V
Stand-by current	I_std	-	-	2.7	μA	Vcc = 3.6V , ST = GND
Symmetry	SYM	45	-	55	%	50% Vcc Level L_CMOS=<15pF
Output voltage	V _{OH}	Vcc-0.4	-	-		-
	V _{OL}	-	-	0.4		-
Output load condition	L_CMOS	-	-	15	pF	CMOS Load
Input voltage	V _{IH}	0.8Vcc	-	-		ST terminal
	V _{IL}	-	-	0.2Vcc		ST terminal
Rise time	t _r	-	-	4	ns	Vcc1.6V : 0.2Vcc to 0.8Vcc Level, L_CMOS=15pF
Fall time	tf	-	-	4	ns	Vcc1.6V : 0.2Vcc to 0.8Vcc Level, L_CMOS=15pF
Start-up time	t_str	-	-	3	ms	t = 0 at 0.9Vcc
Jitter	t _{DJ}	-	0	-	ps	Deterministic Jitter Vcc=3.3V
	t _{RJ}	-	2.4	-	ps	Random Jitter Vcc=3.3V
	t _{RMS}	-	2.3	-	ps	δ(RMS of total distribution) Vcc=3.3V
	t _{p-p}	-	20	-	ps	Peak to Peak Vcc=3.3V
	t _{acc}	-	2.5	-	ps	Accumulated Jitter(δ) n=2 to 50000 cycles
Phase jitter	t _{PJ}	-	0.4	-	ps	Off set Frequency: 12kHz to 20MHz, Vcc=3.3V
Phase noise	L(f)	-	-	-	dBc/Hz	-
		-	-95	-	dBc/Hz	Off set 10Hz Vcc=3.3V
		-	-124	-	dBc/Hz	Off set 100Hz Vcc=3.3V
		-	-146	-	dBc/Hz	Off set 1kHz Vcc=3.3V
		-	-155	-	dBc/Hz	Off set 10kHz Vcc=3.3V
		-	-158	-	dBc/Hz	Off set 100kHz Vcc=3.3V
		-	-159	-	dBc/Hz	Off set 1MHz Vcc=3.3V
Frequency aging	f_age	-3	-	3	x10 ⁻⁶	@+25°C first year
	_	-	-	-		-

3.Timing chart tf tr Vcc 80 % VCC 50 %Vcc 20 %Vcc GND tw 4.Test circuit swich 1) Waveform observation ST VCC by-pass capacito supply Test Point OUT -0 GND L_CMOS 77 2) Current consumption swich VCC ST (A)by-pass capacitor supply OUT 0 *Current consumption under the Test GND Point disable function should be = GND. Ā

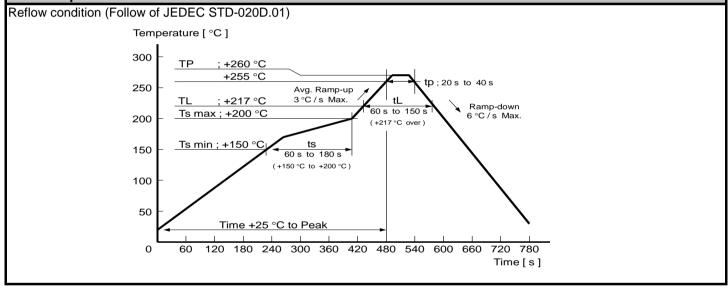
- 3) Condition
- (1) Oscilloscope
- · Band width should be minimum 5 times higher (wider) than measurement frequency.
- · Probe earth should be placed closely from test point and lead length should be as short as possible
- * Recommendable to use miniature socket. (Don't use earth lead.)
- (2) L_CMOS also includes probe capacitance.
- (3) By-pass capacitor (0.01 μF to 0.1 $\mu F)$ is placed closely between VCC and GND.
- (4) Use the current meter whose internal impedance value is small.
- (5) Power supply
- \cdot Start up time (0 %VCC to 90 %VCC) of power source should be more than 150 $\mu s.$
- \cdot Impedance of power supply should be as lowest as possible.





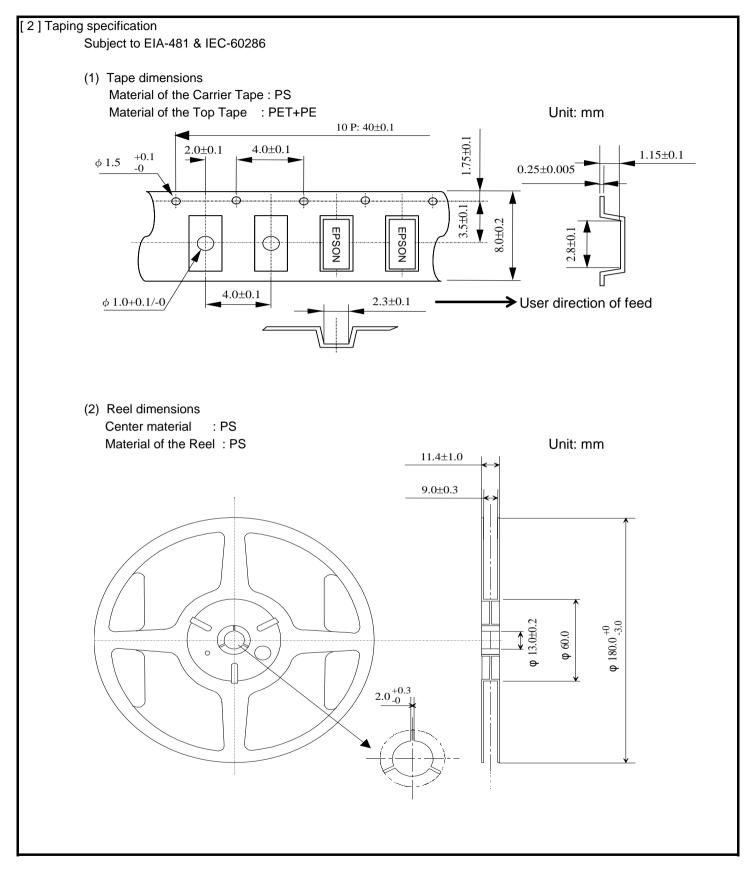
To maintain stable operation, provide a 0.01μ F to 0.1μ F by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc - GND).

7.Reflow profile



8.Packing information

1]Produc	oduct number last 2 digits code(xx) description		The recommended code is "00"		
	X1G0041	710033xx			
	Code	Condition	Code	Condition	
	01	Any Q'ty vinyl bag(Tape cut)	14	1000pcs / Reel	
	11	Any Q'ty / Reel	15	2000pcs / Reel	
	12	250pcs / Reel	00	3000pcs / Reel	



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