

Product name SG5032VAN 100.000000MHz KEGA

Product Number / Ordering code X1G0042610023xx

Please refer to the 9.Packing information about xx (last 2 digits)

Output waveform LVDS

Pb free / Complies with EU RoHS directive

Reference weight Typ. 52 mg

**1.Absolute maximum ratings**

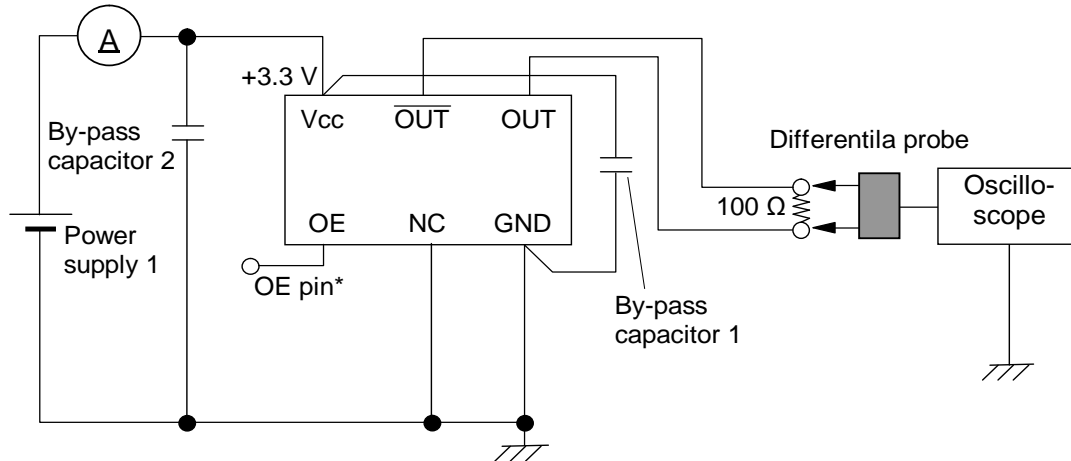
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Maximum supply voltage	Vcc-GND	-0.3	-	+4	V	-
Storage temperature	T_stg	-40	-	+125	°C	Storage as single product
Input voltage	Vin	-0.3	-	Vcc+0.3	V	ST or OE Terminal

**2.Specifications(characteristics)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Output frequency	f <sub>0</sub>	-	100.0000	-	MHz	
Supply voltage	Vcc	2.25	-	3.63	V	-
Operating temperature	T_use	-40	-	+85	°C	-
Frequency tolerance	f_tol	-30	-	30	x10 <sup>-6</sup>	-
Current consumption	I <sub>cc</sub>	-	-	30	mA	OE=Vcc L_LVDS=100 ohm
Stand-by current	I_std	-	-	0.0	mA	-
Disable current	I_dis	-	-	20.0	mA	OE=GND
Symmetry	SYM	45	-	55	%	-
Output voltage(LVDS)	V <sub>OD</sub>	250	-	450	mV	-
	dV <sub>OD</sub>	-	-	50	mV	-
	V <sub>OS</sub>	1.15	-	1.35	V	-
	dV <sub>OS</sub>	-	-	150	mV	-
Output load condition(LVDS)	L_LVDS	-	100	-	Ω	-
Input voltage	V <sub>IH</sub>	0.7Vcc	-	-		-
	V <sub>IL</sub>	-	-	0.3Vcc		-
Rise time	t <sub>r</sub>	-	-	300	ps	-
Fall time	t <sub>f</sub>	-	-	300	ps	-
Start-up time	t_str	-	-	3	ms	-
Jitter	t <sub>DJ</sub>	-	8	-	ps	Deterministic Jitter Vcc=2.5V
	T <sub>RJ</sub>	-	2.6	-	ps	Random Jitter Vcc=2.5V
	t <sub>RMS</sub>	-	4.6	-	ps	σ(RMS of total distribution) Vcc=2.5V
	t <sub>p-p</sub>	-	28.5	-	ps	Peak to Peak Vcc=2.5V
	t <sub>acc</sub>	-	-	-	ps	-
Phase jitter	t <sub>pJ</sub>	-	0.32	-	ps	Off set Frequency: 12kHz to 20MHz Vcc=2.5V
Phase noise	L(f)	-	-	-	dBc/Hz	-
		-	-77	-	dBc/Hz	Off set 10Hz Vcc=2.5V
		-	-109	-	dBc/Hz	Off set 100Hz Vcc=2.5V
		-	-125	-	dBc/Hz	Off set 1kHz Vcc=2.5V
		-	-135	-	dBc/Hz	Off set 10kHz Vcc=2.5V
		-	-141	-	dBc/Hz	Off set 100kHz Vcc=2.5V
		-	-142	-	dBc/Hz	Off set 1MHz Vcc=2.5V
Frequency aging	f_age	-5	-	5	x10 <sup>-6</sup> /Year	25°C,1stYear
		-	-	-		-

### 3. Test circuit

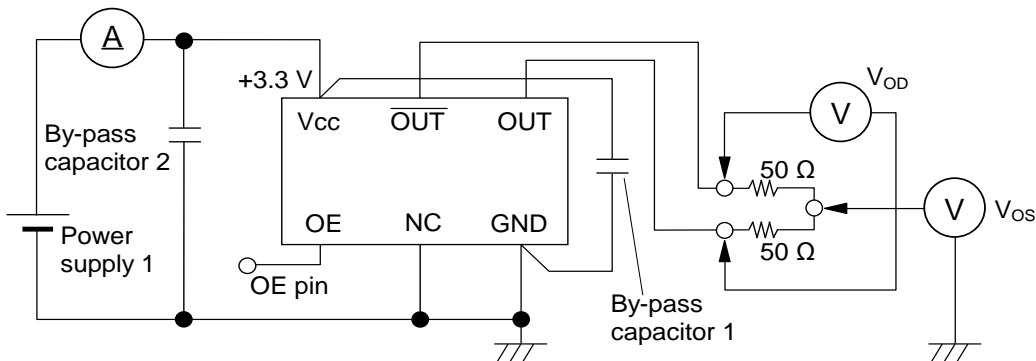
1) To observe waveform and current (case 1)



\* The lines from OUT and  $\overline{\text{OUT}}$  pin are same length.

\* To measure the disable current, OE pin is connected to GND

2) To observe waveform and current (case 2)



\* The lines from OUT and  $\overline{\text{OUT}}$  pin are same length.

3) Measurement condition

A) Oscilloscope

- Bandwidth should be 5 times higher than DUT's output frequency (4 GHz).
- Probe ground should be placed closely from test point and lead length should be as short as possible.

B) By-pass capacitor 1 (approx. 0.01  $\mu\text{F}$  to 0.1  $\mu\text{F}$ ) places closely between Vcc and GND.

C) By-pass capacitor 2 (approx. 10  $\mu\text{F}$ ) places closely between power supply terminals on the board.

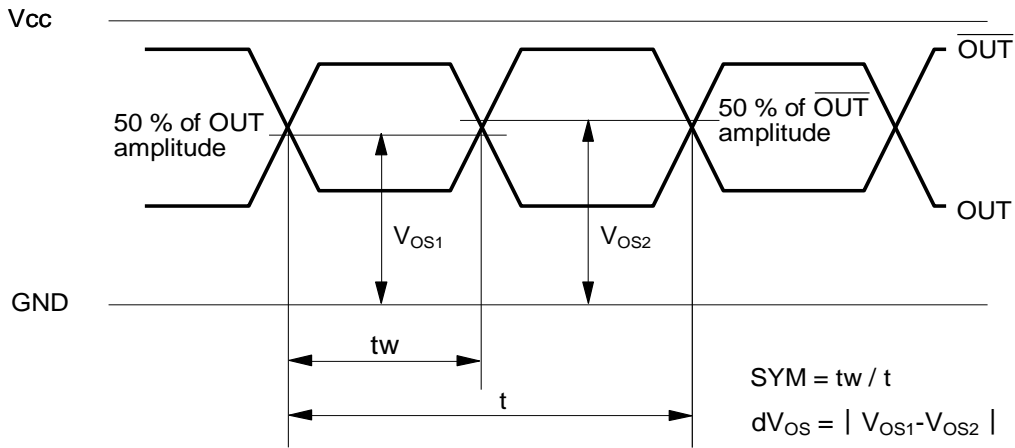
D) Use the current meter whose internal impedance value is small.

E) Power supply

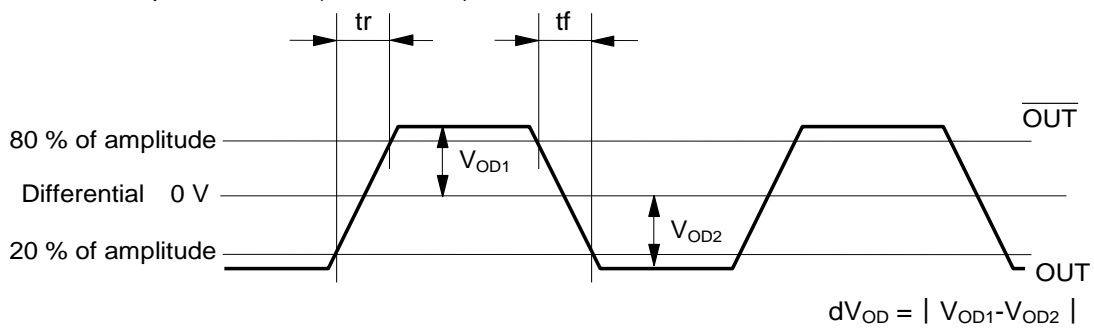
- Start up time (0 Vg90 %Vcc) of power source should be more than 150  $\mu\text{s}$  and slew rate should be less than 19.8 mV/ $\mu\text{s}$ .
- Impedance of power supply should be as low as possible.

### 4. Timing chart

Each output waveform (OUT, and  $\overline{\text{OUT}}$ )



Differential output waveform (OUT -  $\overline{\text{OUT}}$ )



#### 5. External dimensions (Unit: mm)

Pin	Connection
1	OE
2	N.C.
3	GND
4	OUT
5	$\overline{\text{OUT}}$
6	VCC

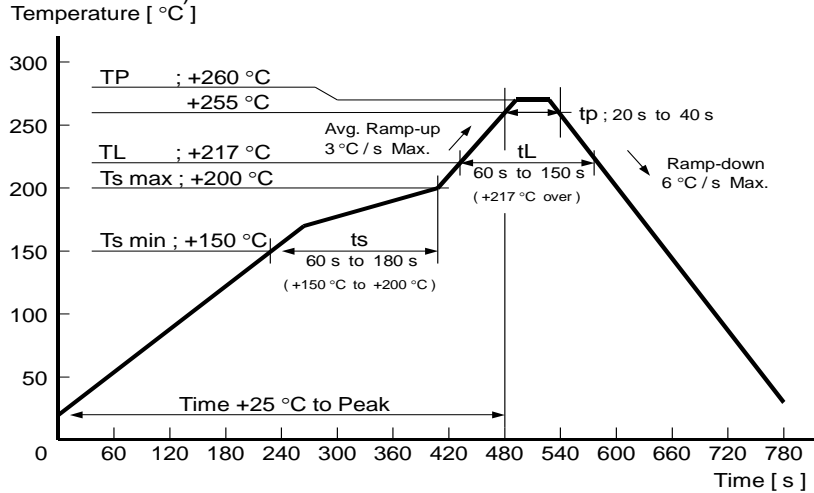
OE pin = HIGH : Specified frequency output  
 OE pin = LOW : Output is high impedance  
 #3 is connected to the cover.  
 Not to scale.

#### 6. Footprint (Recommended) (Unit: mm)

To maintain stable operation, provide a 0.01 $\mu$ F to 0.1 $\mu$ F by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc - GND).

**7.Reflow profile**

Reflow condition (Follow of JEDEC STD-020D.01)

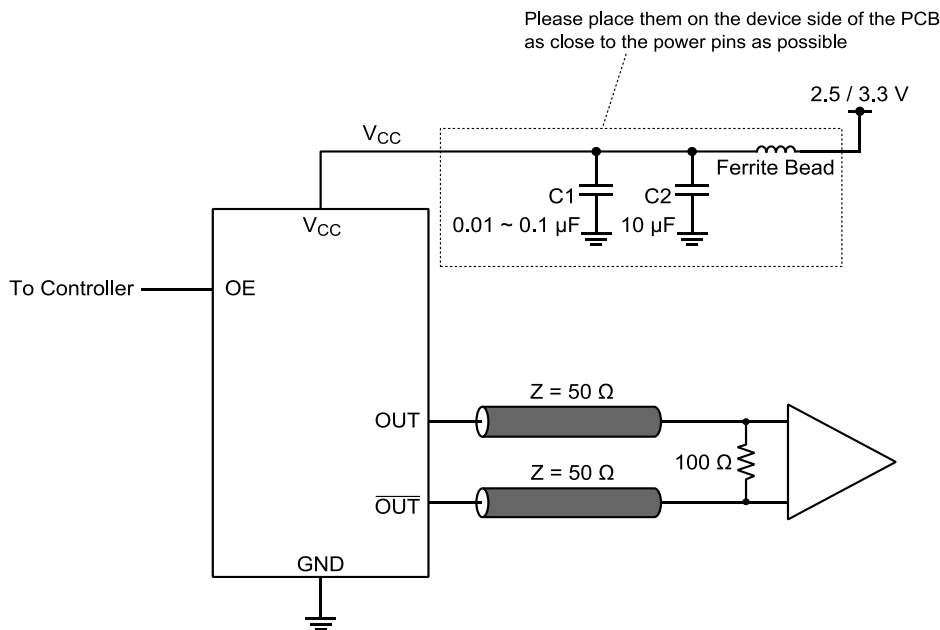


**8.Example of schematic layout**

This figure shows an example of this product's application schematic.

As with any high speed analog circuitry, the power supply pins for this device are vulnerable to noise. In order to achieve optimum jitter performance, power isolation with filter device is required for power supply pins.

In order to achieve best performance of the power isolation filter, it is recommended that the filter composing devices is placed on the device side of the PCB as close to the power pins as possible.





[ 2 ] Taping specification

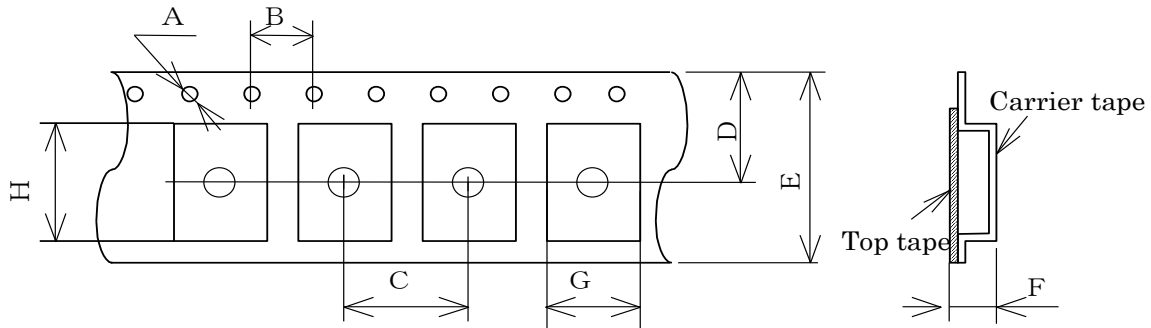
Subject to EIA-481 & IEC-60286

(1) Tape dimensions

Material of the Carrier Tape : PS

Material of the Top Tape : PET+PE

Unit: mm

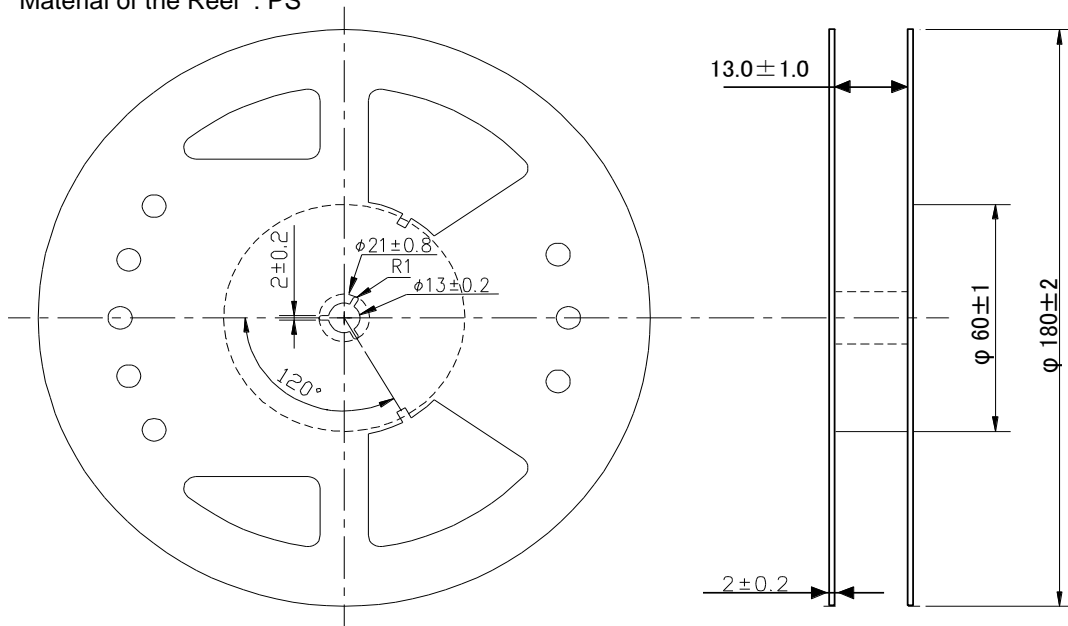


Symbol	A	B	C	D	E	F	G	H
Value	$\phi 1.5$ $+0.1/-0$	$4.0 \pm 0.1$	$8.0 \pm 0.1$	$7.25 \pm 0.2$	$12.0 \pm 0.2$	$1.40 \pm 0.1$	$3.5 \pm 0.1$	$5.4 \pm 0.1$

(2) Reel dimensions

Center material : PS

Material of the Reel : PS



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